AMENDMENTS TO THE CLAIMS

1. (ORIGINAL) A method for testing a network switch chip having an expansion

port configured for transferring data according to a prescribed protocol, the method comprising:

receiving by an external logic unit an expansion port frame from the expansion port via

an expansion bus;

generating by the external logic unit a new expansion port frame based on reception of

the expansion port frame; and

outputting the new expansion port frame onto the expansion bus for reception by the

expansion port of the network switch chip.

2. (ORIGINAL) The method of claim 1, wherein the generating step includes

changing data within the received expansion port frame to generate the new expansion port

frame.

3. (ORIGINAL) The method of claim 2, wherein the changing step includes:

parsing a header of the expansion port frame to retrieve a source address value from a

source address field and a destination address value from a destination address field;

inserting the source address value into the destination address field, and the destination

address value into the source address field, of the new expansion port frame.

4. (ORIGINAL) The method of claim 3, wherein the changing step further includes

inserting a new device identifier value, different from a value of an existing device identifier

value in the received expansion port frame, into a device identifier field in the new expansion

port frame.

5. (ORIGINAL) The method of claim 4, wherein the external logic unit is

implemented using a field programmable gate array.

6. (ORIGINAL) The method of claim 1, wherein the external logic unit is

implemented using a field programmable gate array.

7. (CURRENTLY AMENDED) A test system for testing a network switch chip

having an expansion port configured for transferring data according to a prescribed protocol, the

system comprising:

an expansion port bus configured for propagation of the expansion port frame having

been output by the expansion port; and

an external logic unit configured for generating a new expansion port frame based on

reception of the expansion port frame, and outputting the new expansion port frame onto the

expansion bus for reception by the expansion port of the network switch chip.

8. (ORIGINAL) The system of claim 7, wherein the external logic unit is configured

for generating the new expansion port frame by changing data within the received expansion port

frame.

9. (ORIGINAL) The system of claim 8, wherein the external logic unit is configured

for changing data by parsing a header of the expansion port frame to retrieve a source address

value from a source address field and a destination address value from a destination address field,

the external logic unit inserting the source address value into the destination address field, and

the destination address value into the source address field, of the new expansion port frame.

10. (ORIGINAL) The system of claim 9, wherein the external logic unit is configured

for inserting a new device identifier value into a device identifier field in the new expansion port

frame.

11. (ORIGINAL) The system of claim 7, wherein the external logic unit is

implemented using a field programmable gate array.

12. (NEW) The method of claim 1, wherein the receiving of the expansion port frame

includes:

asserting by the external logic unit an expansion port receiver request signal, on a

corresponding signal path of the expansion bus, to enable the expansion port of the network

switch chip to output the expansion port frame onto a single expansion port transmit data path of

the expansion bus, the external logic unit asserting the expansion port receiver request signal

until detecting a buffer of the external logic unit has been filled; and

storing into the buffer, during assertion of the expansion port receiver request signal,

frame data of the expansion port frame received in prescribed bursts via the single expansion port

transmit data path based on a first clock signal received from the expansion port via a

corresponding first clock path of the expansion bus.

13. (NEW) The method of claim 12, wherein the outputting of the new expansion port

frame includes:

receiving by the external logic unit a second expansion port receiver request signal from

the expansion port via a corresponding signal path of the expansion bus; and

outputting second frame data, in response to receiving the second expansion port receiver

request signal, in prescribed bursts via a single expansion port receive data path of the expansion

bus, according to a second clock signal output by the external logic unit onto a corresponding

second clock path of the expansion bus.

14. (NEW) The method of claim 13, wherein the step of outputting second frame data

includes outputting, onto a corresponding signal path of the expansion bus, a start of burst signal

indicating the single expansion port receive data path carries a corresponding burst of valid data.

15. (NEW) The method of claim 14, wherein the receiving of the expansion port frame

further includes receiving, from a corresponding signal path of the expansion bus, a second start

of burst signal indicating the single expansion port transmit data path carries a corresponding

burst of valid data.

16. (NEW) The test system of claim 7, further comprising a buffer, and wherein:

the external logic unit is configured for asserting an expansion port receiver request

signal, on a corresponding signal path of the expansion bus, to enable the expansion port of the

network switch chip to output the expansion port frame onto a single expansion port transmit

data path of the expansion bus, the external logic unit asserting the expansion port receiver

request signal until detecting the buffer has been filled; and

the expansion port frame being received, during assertion of the expansion port receiver

request signal, as frame data in prescribed bursts via the single expansion port transmit data path

based on a first clock signal received from the expansion port via a corresponding first clock path

of the expansion bus.

17. (NEW) The test system of claim 16, wherein the external logic unit, in response to

receiving a second expansion port receiver request signal from the expansion port via a

corresponding signal path of the expansion bus, is configured for outputting the new expansion

port frame as second frame data in prescribed bursts via a single expansion port receive data path

of the expansion bus, according to a second clock signal output by the external logic unit onto a

corresponding second clock path of the expansion bus.

18. (NEW) The test system of claim 17, wherein the external logic unit is configured

for outputting, onto a corresponding signal path of the expansion bus, a start of burst signal

indicating the single expansion port receive data path carries a corresponding burst of valid data.

19. (NEW) The test system of claim 18, wherein the external logic unit is configured for

receiving, from a corresponding signal path of the expansion bus, a second start of burst signal

indicating the single expansion port transmit data path carries a corresponding burst of valid data.

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